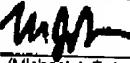


I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail, in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on the date shown below.

Dated: January 30, 2002

Signature: 
(Michael J. Doherty)No.: TESSERA 3.0-085 CONT DIV CONT
(PATENT)

#9
Amendment
J. W. L.
J-22-07

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Joseph Fjelstad

Application No.: 09/784,965

Group Art Unit: 2811

Filed: February 16, 2001

Examiner: A. Chambliss

For: MICROELECTRONIC ASSEMBLIES
HAVING EXPOSED CONDUCTIVE
TERMINALS (As Amended)

Commissioner for Patents
Washington, DC 20231

AMENDMENT

Dear Sir:

In response to the Office Action mailed July 30, 2001, please amend the above-identified application as follows:

IN THE SPECIFICATION

CLEAN COPY OF AMENDED SPECIFICATION PARAGRAPHS:

Please delete the title presently on file, and insert therefore the following title:

--MICROELECTRONIC ASSEMBLIES HAVING EXPOSED CONDUCTIVE TERMINALS--

IN THE DRAWINGS

Please amend drawing FIG. 3 as indicated in the attached letter to the Official Draftsman.

IN THE CLAIMS

CLEAN COPY OF AMENDED CLAIMS:

A2

1. (Amended) A microelectronic assembly comprising:
a microelectronic element having a front face including contacts, a back surface remote therefrom and edges extending therebetween;

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A2
 a mass of a dielectric material at least partially encapsulating said microelectronic element;

(6h)
 conductive units embedded in said mass of dielectric material along at least one microelectronic element edge, at least some of said conductive units being exposed on oppositely-facing exterior surfaces of said mass of dielectric material, wherein at least some of said conductive units include pad portions exposed at said bottom surface of said dielectric material and a protrusion extending from said pad portion, said protrusion being exposed at said top surface of said dielectric material, wherein each of said protrusions extends from a portion of the associated pad portion furthest from said microelectronic element; and

conductive elements extending through said mass of dielectric material and electrically interconnecting said contacts with said conductive units.

A3
 3. (Amended) The assembly as claimed in claim 2, wherein the cross sectional area of each said protrusion is smaller than the cross sectional area of the pad portion associated with such protrusion.

A4
 13. (Amended) The assembly as claimed in claim 12, wherein said reflowable material is exposed at at least one exterior surface of the assembly.

14. (Amended) A microelectronic assembly comprising:
 a first microelectronic element having a front face including contacts and a back surface remote therefrom;

a second microelectronic element juxtaposed with said front face of said first microelectronic element and having terminals thereon;

a continuous mass of a dielectric material at least partially encapsulating said first microelectronic element and fully encapsulating said second microelectronic element; *wherein said*

conductive units secured to said continuous mass of dielectric material; and

conductive elements extending through said continuous mass of dielectric material and electrically interconnecting said contacts and said terminals with said conductive units or with each other, wherein one or more of said conductive units are exposed at an exterior surface of said assembly.

A5
 18. (Amended) The assembly as claimed in claim 14, wherein said conductive elements interconnect at least one of said terminals to at least one of said contacts.

~~Please cancel claims 4, 21-23.~~

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MARKED-UP COPY OF AMENDED CLAIMS:

1. (Amended) A microelectronic assembly comprising:
a microelectronic element having a front face including contacts, a back surface remote therefrom and edges extending therebetween;
a mass of a dielectric material at least partially encapsulating said microelectronic element;

conductive units embedded in said mass of dielectric material along at least one microelectronic element edge, at least some of said conductive units being exposed on oppositely-facing exterior surfaces of said mass of dielectric material, wherein at least some of said conductive units include pad portions exposed at said bottom surface of said dielectric material and a protrusion extending from said pad portion, said protrusion being exposed at said top surface of said dielectric material, wherein each of said protrusions extends from a portion of the associated pad portion furthest from said microelectronic element; and

conductive elements extending through said mass of dielectric material and electrically interconnecting said contacts with said conductive units.

3. (Amended) The assembly as claimed in claim 2, wherein at least some of said conductive units include pad portions exposed at said bottom surface of said dielectric material and a protrusion extending from said pad portion exposed at said top surface of said dielectric material, wherein the cross sectional area of each said protrusion is smaller than the cross sectional area of the pad portion associated with such protrusion.

13. (Amended) The assembly as claimed in claim 12, wherein said reflowable material is exposed at at least one exterior surface of the assembly.

14. (Amended) A microelectronic assembly comprising:
a first microelectronic element having a front face including contacts and a back surface remote therefrom;
a second microelectronic element juxtaposed with said front face of said first microelectronic element and having terminals thereon;
a continuous mass of a dielectric material at least partially encapsulating said first microelectronic element and fully encapsulating said second microelectronic element;
conductive units secured to said continuous mass of dielectric material; and
conductive elements extending through said continuous mass of dielectric material and electrically interconnecting said contacts and said terminals with said conductive

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units and/or with each other, wherein one or more of said conductive units are exposed at an exterior surface of said assembly.

18. (Amended) The assembly as claimed in claim 17 14, wherein said conductive elements interconnect at least one of said terminals to at least one of said contacts.

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REMARKS

The present Amendment is in response to the Office Action mailed July 30, 2001, in the above-identified patent application. A petition requesting a three-month extension of time for responding to the Office Action from October 30, 2001 to and including January 30, 2002, is enclosed herewith.

The Examiner objected to the title as being not descriptive of the claimed invention. In response, Applicant has amended the title as suggested by the Examiner.

The Examiner objected to the drawings as failing to comply with 37 C.F.R. § 1.84(p)(4). In response, FIG. 3 has been amended, as indicated in the attached Letter to the Official Draftsman.

The Examiner objected to claims 3 and 18 as having informalities. In response, Applicant has amended claim 3 to delete "top surface of said dielectric material" therefrom, thereby rendering the Examiner's objection moot. Claim 18 has been amended as suggested by the Examiner.

Claims 1-4 and 7-8 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 5,844,315 to *Melton et al.* Referring to FIGS. 4-7 thereof, *Melton* discloses a microelectronic package 10 including a chip 12 having contacts 36 that are electrically interconnected with metallic leads 16 by wire lead 18. Metallic bumps 20 are formed atop metallic leads 16 and a layer of a polymeric material 21 encapsulates chip 12 and wire leads 18. The tops 30 of the metallic bumps 20 are exposed at a top surface of the polymeric layer 21 and the metallic leads 16 are exposed at a bottom surface of the polymeric layer 21. The metallic leads 16 extend outwardly from the metallic bumps 20.

As an initial matter, Applicant notes that claim 1 has been amended to incorporate limitations from claims 3 and 4 therein.

As amended, claim 1 is unanticipated by *Melton* because the cited reference neither discloses nor suggests a microelectronic assembly, "wherein at least some of said units include pad portions exposed at said bottom surface of said dielectric material and a protrusion extending from said pad portion, said protrusion being exposed at said top surface of said dielectric

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material, wherein each of said protrusions extends from a portion of the associated pad portion furthest from said microelectronic element." This feature is clearly shown in Applicant's FIG. 3 wherein conductive pad 110' includes a protrusion 116' that extends from a portion of the conductive pad furthest from the microelectronic element.

Claim 2 is unanticipated, *inter alia*, by virtue of its dependence from claim 1, which is unanticipated for the reasons set forth above.

Claim 3 is unanticipated because *Melton* does not teach a microelectronic assembly "wherein the cross-sectioned area of each said protrusion is smaller than the cross-sectional area of the pad portion associated with such protrusion." Referring to FIG. 3 thereof, *Melton*'s lead 16 has a greater cross-sectional area than bump 20 formed on the lead 16.

Claim 4 has been cancelled, thereby rendering the rejection moot.

Claims 7 and 8 are unanticipated, *inter alia*, by virtue of their dependence from claim 1, which is unanticipated for the reasons set forth above.

The Examiner also rejected claims 5-6, 10-12, 14, 18 and 20 under 35 U.S.C. § 103(a) as being unpatentable over *Melton* in view of U.S. Patent 5,608,265 to *Kitano et al.* Referring to FIGS. 1 and 2 thereof, *Kitano* discloses a package including a semiconductor chip 1 having contacts. The chip 1 is mounted on a chip pad 2, and the chip contacts are electrically connected with leads 4 by metallic wires 3. The package is encapsulated with a resinous mass 6 having holes extending from a solder pad to both surfaces of the package. A solder bump 5 connected to the solder pad is provided inside the holes. As shown in FIG. 1, a tip 5A of the solder bump is shown projecting on the package surface. As shown in FIG. 2, the solder bumps 5 connected to the solder pads 4-1, 4-2 and 4-3 provided within holes 7 are connected to a wiring pattern 9 provided on a printed circuit board 8. Any embodiment shown in FIG. 10, four semiconductor devices are placed one atop another with the respective leads 4 connected by bumps 5. In response, Applicant respectfully notes that *Kitano* does not overcome the deficiencies noted above in *Melton*.

Claims 5-6 and 10-12 are unobvious, *inter alia*, by virtue of their dependence either directly or indirectly from claim 1, which patentable for the reasons set forth above.

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The limitations of claim 14 are shown in Applicant's FIG. 4B, whereby a microelectronic package includes two chips encapsulated in a single, continuous layer of a dielectric material. Specifically, the microelectronic package of FIG. 4B includes a first chip 120", a second chip 170" mounted atop first chip 120", with a single, continuous layer of a dielectric material encapsulating both chips 120" and 170".

Claim 14, as amended, is unobvious over the combination of *Melton* and *Kitano* because the references neither disclose nor suggest a microelectronic assembly including "a continuous mass of a dielectric material at least partially encapsulating said first microelectronic element and fully encapsulating said second electronic element."

Claims 18 and 20 are unobvious by virtue of their dependence from claim 14, which is unobvious for the reasons set forth above.

The Examiner rejected claims 14-19 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 5,608,265 to *Kitano*. As noted above, *Kitano* (FIG. 10) shows a package having four (4) separate layers of a dielectric material with gaps between each layer. The layers of dielectric material are not "continuous." Thus, *Kitano* does not teach the structure shown in Applicant's FIG. 4B and claimed in claim 14, namely, a microelectronic assembly including "a continuous mass of a dielectric material at least partially encapsulating said first microelectronic element and fully encapsulating said second microelectronic element; conductive units secured to said continuous mass of dielectric material; and conductive elements extending through said continuous mass of dielectric material and electrically interconnecting said contacts and said terminals with said conductive units." (Emphasis added)

Claims 15-19 are also unanticipated, *inter alia*, by virtue of their dependence from claim 14, which is unanticipated by the reasons set forth above.

Claims 21-23, withdrawn from consideration by the Examiner, have been cancelled.

As it is believed that all of the rejections, objections and requirements set forth by the Examiner have been satisfied, prompt and favorable allowance of the present application is earnestly solicited.

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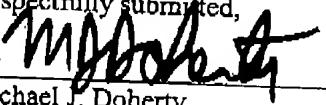
If, however, for any reason the Examiner does not believe that such action can be taken at this time, it is respectfully requested that he telephone Applicant's attorney at (908) 654-5000 in order to overcome any additional objections which he might have.

If there are any additional charges in connection with this requested amendment, the Examiner is authorized to charge Deposit Account No. 12-1095 therefor.

Dated: January 30, 2002

Respectfully submitted,

By


Michael J. Doherty

Registration No.: 40,592

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